

# **TC285 Application Note**

## **Introduction**

**This Application Note describes the steps required to optimize the clock levels of the TC285SPD for best possible image quality. The assumption is that suitable driver circuits have already been designed. There are recommended circuit drawings in the TC285SPD data sheet.**

**All clock levels must be controllable.**

## **Procedure**

1. Initial Set Up
2. Optimization of CMG LOW Level
3. Optimization of RST HIGH Level
4. Optimization of SRG1/SRG2 HIGH Level(s)
5. Fine Adjustment of SRG1 HIGH Level
6. Multiplication Gain Measurement
7. Optimization of ODB LOW Level and IAG1/IAG2/SAG1/SAG2 HIGH Levels
8. Fine Adjustment of IAG/SAG High Levels
9. Optimization of ODB HIGH Level

## 1. Initial Set Up

Please set all clock levels to the corresponding “NOM” values in latest data sheet. If you can’t get a functional image under those bias conditions, please verify clock timing and confirm connections.

Further clock level optimization described in this application note should be controlled within the range of the “MAX” and “MIN” values defined in “recommended operating conditions” of TC285 data sheet.

\*Note that the current data sheet is for the prototype version, “TX285”. Both the current data sheet and this application note are “Preliminary”. The actual “MAX” and “MIN” values have not yet been determined, and what is listed is meant as a guideline. The values of these parameters are subject to change in the final product.

## 2. Optimizing CMG LOW Level

Increase the CMG HIGH level to get about 1000x multiplication gain and shield the light to get a dark image.

(\*refer to section 6 to understand how to get 1000x gain)

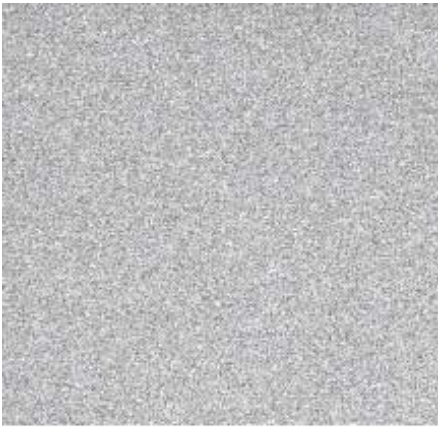


Image-1

**Image-1** is a good reference. **Image- 2** and **Image-3** are examples of bad references.

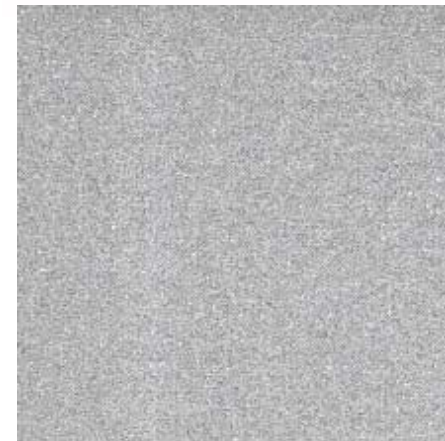


Image-2

If you can see a white vertical belt as shown in **Image-2** or **Image-3**, please lower the CMG LOW level until the white belt diminishes to a negligible level.

If CMG LOW is too negative, the image will disappear. If this happens, raise the CMG LOW voltage level to recover the image.

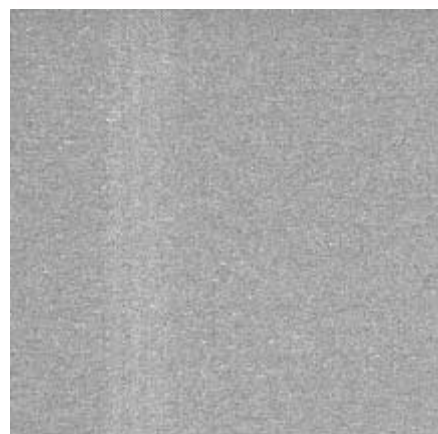


Image-3

### 3. Optimization of RST HIGH Level



*Photo-1*

Use an oscilloscope to monitor the CCD output signal.

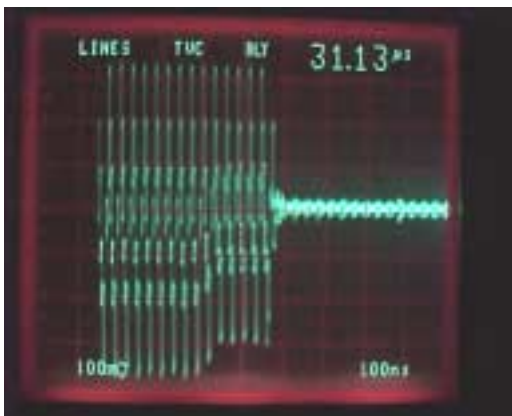
If you don't have a proper H-trigger source available, we recommend using the SAG1 or SAG2 signals as the trigger source.



*Photo-2*

Drop the CMG HIGH level to under 10V. Under this condition, multiplication is not active and gain is equal to 1. Please see the CCD signal shown in *Photo-1*.

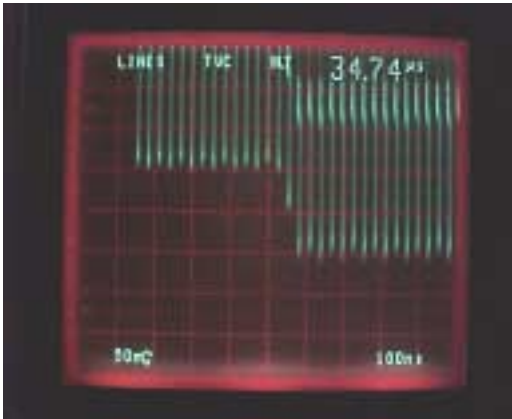
Illuminate the CCD with a uniform flat field, and control the light intensity until the CCD output level becomes about 100mV. We recommend using a viewer to get the flat field.



*Photo-3*

If you detect a step signal at the beginning of the H signal (as indicated by the arrow in *Photo-1*) or at the end of the H signal (as indicated in *Photo-2*), then increase the level of RST HIGH until the step is removed.

## 4. Optimization of SRG1/SRG2 HIGH Level



*Photo-5*

Under the same conditions of illumination and gain as in step-3 (optimization of RST HIGH Level), optimize the SRG1/SRG2 HIGH level(s) (They can be tied together or separate).

As shown in *Photo-5* and *Photo-6*, there is a “half-output-level” pixel at the beginning and at the end of the H signal. Confirm that the output level of the “half-output-level” pixel at the end of the H signal is smaller than 60% of the average signal.



*Photo-6* **Half Pixel**

If it is over 60%, increase the SRG1/SRG2 HIGH level(s) until the output of “half-level-output” pixel becomes smaller than 60% of the average signal.

This adjustment work must be done **AFTER** the optimization of the RST HIGH level.

## 5. Fine Adjustment of SRG1 HIGH Level

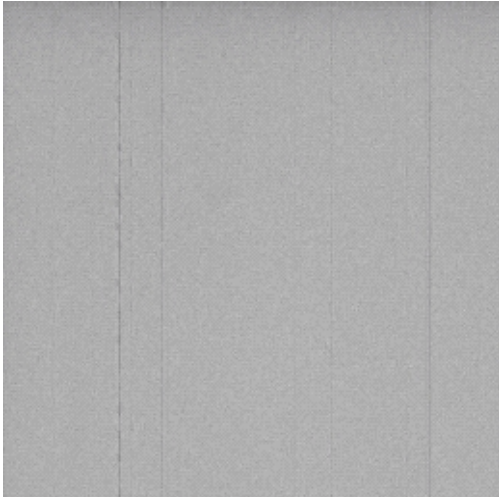


Image-4

Adjust CMG HIGH voltage level to get about 1000x gain (see section 6). Illuminate the CCD with a uniform flat field, and by applying ND filters and/or controlling the iris, adjust until the CCD output level is somewhere between 100 and 300mV.

If you can detect column lines as shown in *Image-4*, please increase the SRG1 HIGH level. If you can't remove these column lines, please check the SAG2 timing during the H-blanking period and try to keep sufficient time from SAG2's falling edge to SRG1's rising edge, as described in data sheet.

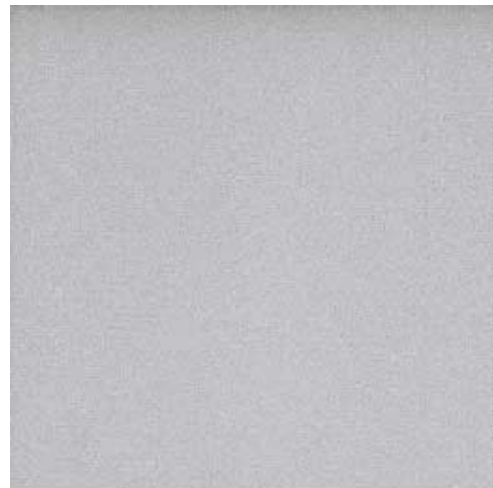


Image-5

(If SRG1 and SRG2 are tied together, then adjust them together, but if they are not, SRG1 is the only one requiring adjustment with respect to vertical-column removal)

## 6. Multiplication Gain Measurement

### Prepare the following tools :

- **Lens** : with at least 8 steps of IRIS control (1<sup>st</sup> step is 100% open)
- **ND filters:** 2 4 8 (additional ones may be needed if no adjustable light source is available)
- **Oscilloscope**

(\* If being referred here by section 2, set CMG LOW to the NOM value as described in the data sheet, and follow the instructions below.)

### Measurement method :

Target a smear chart and keep CMG gain in the “off” condition.

Open the iris fully and adjust the light intensity or apply ND filters (if source is not adjustable) to adjust the CCD output level to around 200mV.

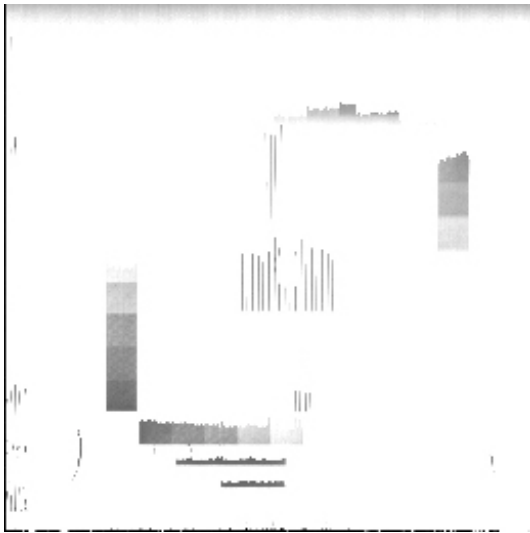
Now, by using the iris and ND filters at increasing CMG HIGH levels, you can map the CMG voltage to actual gain levels. For example, 1 step of the iris will reduce the light to the camera by half, the next step by half again, and so on... When the 8-step iris is fully closed, the light level will have been reduced by a factor of  $2^7 = 128$  from the fully open position. By turning the CMG HIGH voltage level up until the output voltage reaches the same level it was prior to light reduction (i.e. around 200mV), we can assign that CMG HIGH voltage level to a corresponding gain of 128x. To map gains higher than that, ND filters can be used in combination with the fully closed iris as shown in the table below.

Gain	ND2	ND4	ND8
256	○		
512		○	
1024			○
2048	○		○

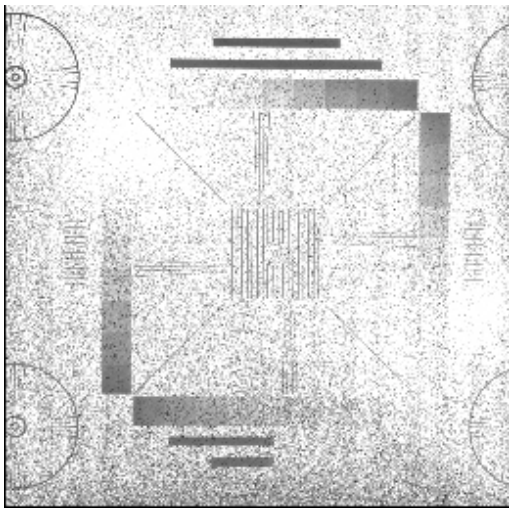
## 7. Optimization of ODB LOW Level and IAG1/IAG2/SAG1/SAG2 HIGH Levels

We recommend designing the circuit to clip the CCD output at white level saturation point of 200mV, when multiplication is off.

Drop the CMG HIGH level to lower than 10V to keep CMG gain at 1. Put a resolution chart on the viewer and open the iris to saturate in the white areas of the image chart. Then open the iris 3 steps (8x brightness). If the image looks like *Image-6*, no adjustment is needed for ODB LOW or for IAG/SAG HIGH.



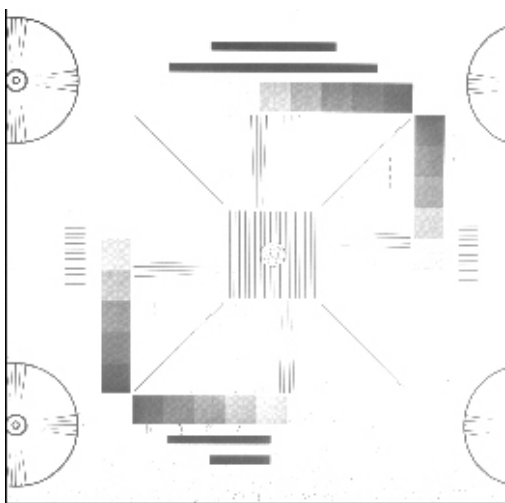
**Image-6**



**Image-7**

If the image shows blooming on the gray bars as in *Image-6*, however, increase the ODB LOW level until you get a “sandy” image as in *Image-7*. Going that high is just to confirm the upper limit of ODB LOW. Now reduce the ODB LOW level slightly until the “sand” disappears.

If blooming remains, increase the HIGH levels of IAG1/IAG2/SAG1/SAG2 until eliminating blooming as shown in *Image-8*.



**Image-8**

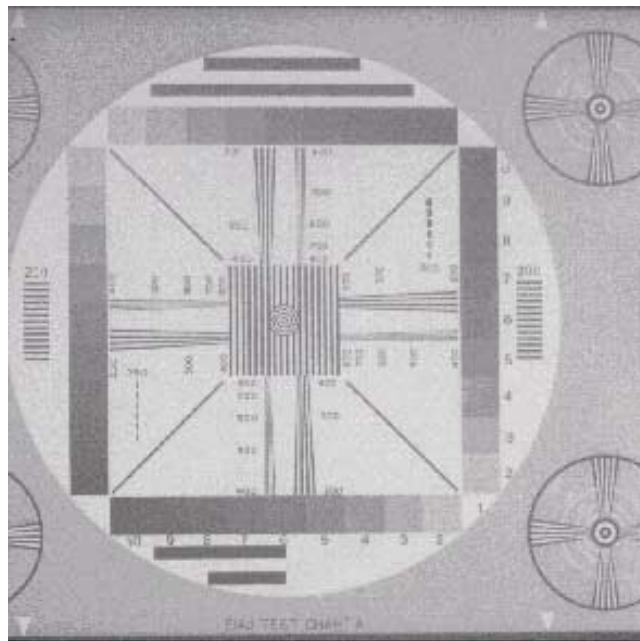
The following conditions should be maintained during the optimization work.

$$\begin{aligned} \text{IAG1} < \text{IAG2} \text{ and} \\ \text{SAG1} < \text{SAG2} \end{aligned}$$

From a noise-performance point of view, all clock voltage should be optimized as low as possible.

## 8. Fine Adjustment of IAG/SAG HIGH Levels

Adjust the CMG HIGH level to get about 1000x gain.  
Attenuate the light intensity using the iris and ND filters and target a resolution chart as shown below.  
If you don't see reasonable vertical resolution (i.e. 700-800 lines) then increase IAG/SAG HIGH slightly.



## 9. Optimization of ODB HIGH Level PART I

When using the electric shutter function, the following adjustments are necessary.

Set exposure time to over 33ms.

Adjust the CMG HIGH level to get about 1000x gain and target a bright square, as shown in *Image-9*, to use as your smear chart

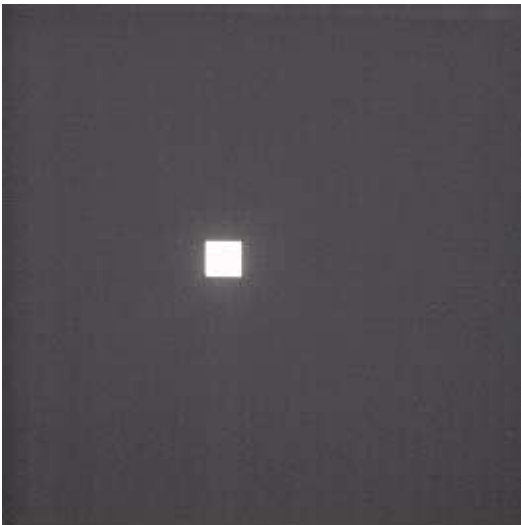


Image-9

Set the minimum shutter time for your system. If you see blooming on the upper side of the square, for example as in *Image-10*, please increase the ODB HIGH level until it diminishes to a negligible level.

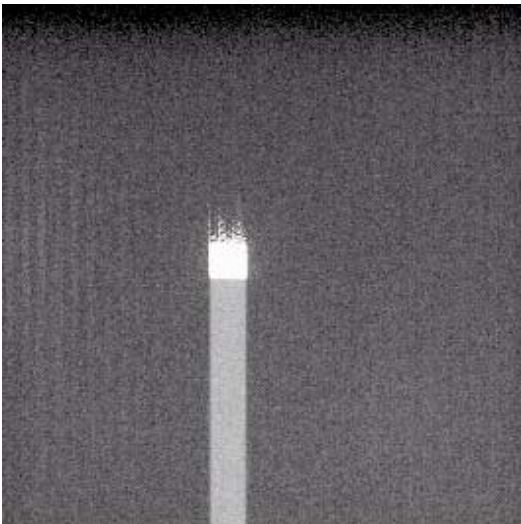


Image-10

With optimization of the ODB HIGH level, the smear chart should begin to appear as it does in *Image-11*.

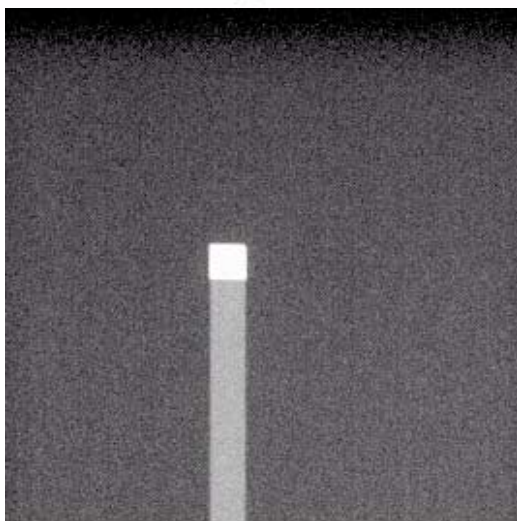


Image-11

## 9) cont...Optimization of ODB HIGH Level PART II

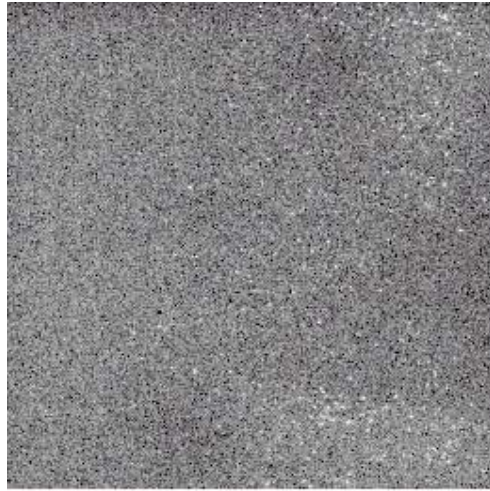


Image-12

If the ODB HIGH bias is over the voltage limit defined as the maximum level in data sheet, You will see a lot of white dots all over the image as shown in *Image-12*.

If this occurs, please drop the ODB HIGH level until white dots disappear.